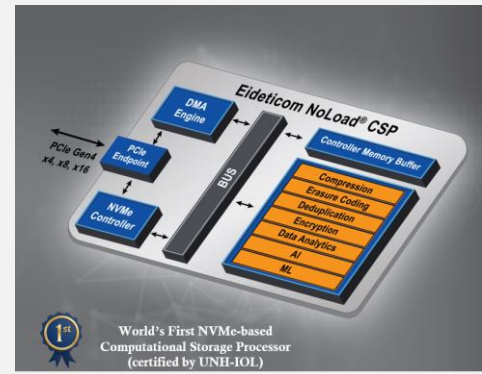
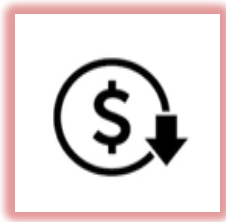


Transparent Compression using NoLoad[®] Computational Storage Processor



Eideticom's NoLoad CSP provides hardware-based compression that enables **increased capacity (lower \$/GB) without sacrificing performance**



Reduced Cost

- Increased Storage Capacity
- Reduced Server Count
- Better NAND Lifetime



Higher Performance

- Maximum CPU Offload
- Best Application Performance
- Superior Quality of Service (QoS)



Lower Power

- Increased CPU Efficiency
- Reduced CPU Count
- Relaxed CPU Load

90% Lower Total Cost

2x Throughput Per Server

60% Lower Power



2 Dual-CPU Servers

10.7 GB/sec Compression Throughput
278TB effective (192TB SSDs)

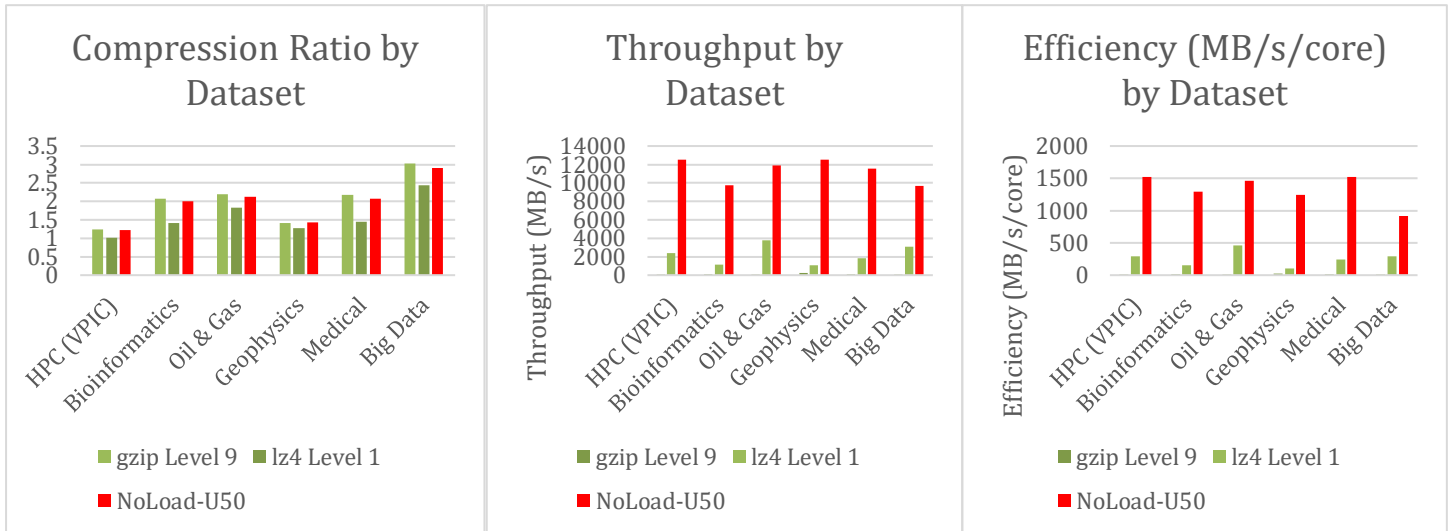
 EIDETICOM
NoLoad Acceleration



1 Single-CPU Server (+2 NoLoad)

23 GB/sec Compression Throughput
400TB effective (192TB SSDs)

Solution Brief: Transparent Compression using NoLoad® CSP



Cost-Benefit Analysis

- **Storage Capacity Costs:** NoLoad Compression reduces the effective \$/GB of the system by increasing the amount of data that can be stored on SSDs.
- **Storage Lifetime Costs:** NoLoad's higher Compression Ratio (CR) extends the lifetime of an SSD, since for a given compression input throughput it reduces the Drive Writes Per Day (DWPD).
- **Throughput Performance Costs:** NoLoad compression is 3-6 more CPU efficient than lz4-1 and over 100 times more CPU efficient than gzip-9. This enables a smaller CPU with less cores to be utilized and permits a given CPU to run cooler and consume less power since less cores are being loaded.
- **Storage Performance Costs:** NoLoad's increased CR means the write throughput of the SSDs is reduced. This means that cheaper, less performant SSDs can be considered.

NoLoad Hardware

Eideticom NoLoad CSP supports deployment on any PCIe-enabled FPGA card. Two examples are the Xilinx Alveo U50 PCIe-Enabled FPGA card (NoLoad-U50) and the BittWare 250-U2 FPGA Accelerator Card (NoLoad-U2).



“The Eideticom NoLoad devices have demonstrated that we can offload storage functions onto accelerators enabling line-rate compression, improving CPU utilization, and reducing memory bandwidth pressure.”

**Brad Settlemyer, Senior Scientist,
Los Alamos National Laboratory**